**CIS 350 – INFRASTRUCTURE TECHNOLOGIES**

**HOMEWORK #4**

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**Topics**: The CPU and Memory (Chapters 7 and 8)

Ex. Show an instruction format that could be used to move data or perform arithmetic between two registers (the source register and the destination register). Assume that the instruction is 32 bits wide and that the computer has 8 general-purpose registers. If the op code uses 7 bits, how many bits are spares, available for other purposes, such as special addressing techniques? Draw a detailed diagram with the instruction format. Figure 7.21 on p. 228 in your textbook depicting a "register to register" format may be very helpful.

Ex. 7.3, p. 232

Ex. 7.7 a (only), p. 232

Ex. Suppose that the following instructions are found at memory locations 25 and 26. Suppose that the following data are found at memory 55 and 56.

Address Instruction

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25 LDA 55

26 ADD 56 Addresses 25-26 represent the program area

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Data

55 125 Addresses 55-56 represent the data area

56 10

Show the contents of the PC, the MAR, the MDR, the IR, and the A as each step of the fetch-execute cycle is performed for instructions at addresses 25 and 26. (The machine cycle for instruction LDA I worked in class on the white board would be helpful. See page 5 in the lecture notes for chapter 7. I asked students to take notes. Also, look at Assignment One in in-class small group activity #4.)

Instruction: 25 LDA 55

PC MAR MDR IR A

1. PC→ MAR 25 25 LDA 55 ? ?
2. MDR→ IR \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
3. IR[addr] → MAR \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
4. MDR→ A \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
5. PC+1→ PC \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_

Instruction: 26 ADD 56

PC MAR MDR IR A

1. PC→ MAR \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
2. MDR→ IR \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
3. IR[addr] → MAR \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
4. MDR+A→ A \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_
5. PC+1→ PC \_\_\_ \_\_\_ \_\_\_\_\_ \_\_\_\_\_ \_\_\_

**Short essay questions. Your answers should capture the essence of the questions. There is no credit for 1- or 2-sentence answers.**

Ex. 8.4 and 8.5, p. 263.

Ex. 8.16, p. 263. Also briefly explain how cache memory works.

Ex. 8.17, p. 263

Ex. 8.18, p. 263